CLAIMS

What is claimed is:

1. A semiconductor integrated circuit comprising:

a plurality of memory cells connected to a word line;

a row control circuit activating said word line;

a column control circuit performing a read or a write operation in said memory cells selected by said word line being activated;

a command control circuit receiving a column operation command in synchronization with a clock signal and controlling said column control circuit; and

a timing adjusting circuit setting a delay time, which is from the reception of said column operation command to the start of the operation of said column control circuit, to be variable.

2. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit sets said delay time to a predetermined length in accordance with a latency, which is a value equal to the number of clock cycles from said reception of said column operation command to the performance of the read operation or the write operation.

3. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit includes a delay circuit for setting said delay time to a predetermined length.

4. A semiconductor integrated circuit according to claim 1, comprising a latch circuit latching said column operation command received by said command control circuit in response to the receipt of said clock signal delayed by said timing adjusting circuit.

5. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit sets said delay time to a predetermined length in accordance with an operating timing of said row control circuit.

6. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit sets said delay time to a predetermined length for every operation of said row control circuit.

7. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit sets said delay time to a predetermined length in response to the first operation of said row control circuit after the inactive state of an internal circuit.

8. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit sets said delay time to a predetermined length in response to the reception of a refresh command for refreshing said memory cells.

9. A semiconductor integrated circuit according to claim 8, wherein said timing adjusting circuit sets said delay time to a predetermined length in response to the reception of the first refresh command after the power is switched on.

10. A semiconductor integrated circuit according to claim 1, wherein said timing adjusting circuit sets said delay time to a predetermined length in response to a request to adjust said delay time from the exterior.

11. A semiconductor integrated circuit according to claim 1, comprising a mode register for setting an operating mode from the exterior, and wherein

said timing adjusting circuit sets said delay time to a predetermined length in accordance with a value set by said mode register.

12. A semiconductor integrated circuit according to claim 1, comprising a control terminal receiving an external control signal, and wherein

said timing adjusting circuit sets said delay time to a predetermined length in accordance with said control signal fed to said control terminal.

13. A semiconductor integrated circuit comprising:

a plurality of memory cells connected to a bit line;

a precharging circuit setting said bit line to have a predetermined voltage;

a command control circuit receiving a precharge command in synchronization with a clock signal and controlling said precharging circuit; and

a timing adjusting circuit setting a delay time, which

is from the reception of said precharge command to the start of the operation of said precharging circuit, to be variable.

14. A semiconductor integrated circuit according to claim 13, wherein said timing adjusting circuit sets said delay time to a predetermined length in accordance with a latency, which is a value equal to the number of clock cycles from the reception of an operation command to the performance of a read or a write operation.

15. A semiconductor integrated circuit according to claim 14, wherein said timing adjusting circuit includes a delay circuit for setting said delay time to a predetermined length.

16. A semiconductor integrated circuit according to claim 14, comprising a latch circuit latching said precharge command received by said command control circuit in response to the receipt of said clock signal delayed by said timing adjusting circuit.

17. A semiconductor integrated circuit according to claim 14, comprising a row control circuit activating a word line, and wherein

said timing adjusting circuit sets said delay time to a predetermined length in accordance with an operating timing of said row control circuit.

18. A method of controlling a semiconductor integrated circuit, comprising:

a plurality of memory cells connected to a word line;

a row control circuit activating said word line; and

a column control circuit performing a read or a write operation in said memory cells selected by said word line being activated, comprising the step of

setting a delay time, which is from the reception of a column operation command in synchronization with a clock signal, for controlling said column control circuit, to the start of the operation of said column control circuit, to be variable.

19. A method of controlling a semiconductor integrated circuit, comprising:

a plurality of memory cells connected to a bit line and

a precharging circuit for setting said bit line to have a predetermined voltage, comprising the step of

setting a delay time, which is from the reception of a precharge command in synchronization with a clock signal, for controlling said precharging circuit, to the start of the operation of said precharging circuit, to be valuable.

20. A variable delay circuit comprising:

a first delay circuit having a plurality of first delay stages connected in cascade and receiving an input signal at the initial stage of said first delay stages;

a second delay circuit having a plurality of second delay stages identical to said first delay stages, connected in cascade and receiving a first timing signal at the initial stage of said second delay stages;

a detecting circuit detecting, of delayed timing signals outputted from each of said second delay stages, a delayed timing signal having a transition edge near to the transition edge of a second timing signal; and

a selecting circuit selecting a delayed signal outputted from said first delay stage corresponding to said second delay stage outputting said delayed timing signal detected by said detecting circuit.